650V N-ch Planar MOSFET

Lead Free Package and Finish

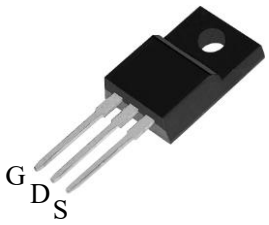
BV_{DSS}	$R_{DS(ON),Typ.}$	I_D
650V	1.2Ω	7.0A

General Features

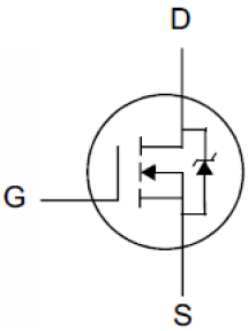
- RoHS Compliant
- $R_{DS(ON),typ.}$=1.2 Ω@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- High surge capability

Applications

- Adaptor
- Charger
- SMPS Standby Power



TO-220F



Package Not to Scale

Ordering Information

Part Number	Package	Brand
PTA07N65G	TO-220F	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	PTA07N65G	Unit
V_{DSS}	Drain-to-Source Voltage	650	V
V_{GSS}	Gate-to-Source Voltage	±30	
I_D	Continuous Drain Current @ T_C = 25ºC	7	A
	Continuous Drain Current @ T_C = 100ºC	4.4	
I_{DM}	Pulsed Drain Current at V_{GS}=10V	28	
E_{AS}	Single Pulse Avalanche Energy	700	mJ
P_D	Power Dissipation	46	W
	Derating Factor above 25℃	0.31	W/℃
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTA07N65G	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.7	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	

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Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	650	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=650V, V_{GS}=0V
		--	--	100		V_{DS}=520V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	1.20	1.38	Ω	V_{GS}=10V, I_D=3.5A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	1282	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	2.8	--		
C_{oss}	Output Capacitance	--	87	--		
Q_g	Total Gate Charge	--	20.5	--	nC	V_{DD}=325V, I_D=7A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	6.4	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	5.8	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$td_{(ON)}$	Turn-on Delay Time	--	13.9	--	ns	V_{DD}=325V, I_D=7A, V_{GS}=10V Rg=25Ω
t_{rise}	Rise Time	--	3.15	--		
$td_{(OFF)}$	Turn-Off Delay Time	--	21.8	--		
t_{fall}	Fall Time	--	7.1	--		

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Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current[2]	--	--	7	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current[2]	--	--	28		
V_{SD}	Diode Forward Voltage	--	--	1.4	V	I_S=7A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	752	--	ns	V_{GS}=0V I_F=7A, di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	4.5	--	uC	

Note:

[1] T_J=+25℃ to +150℃
[2] Pulse width≤380μs; duty cycle≤2%.

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Typical Characteristics

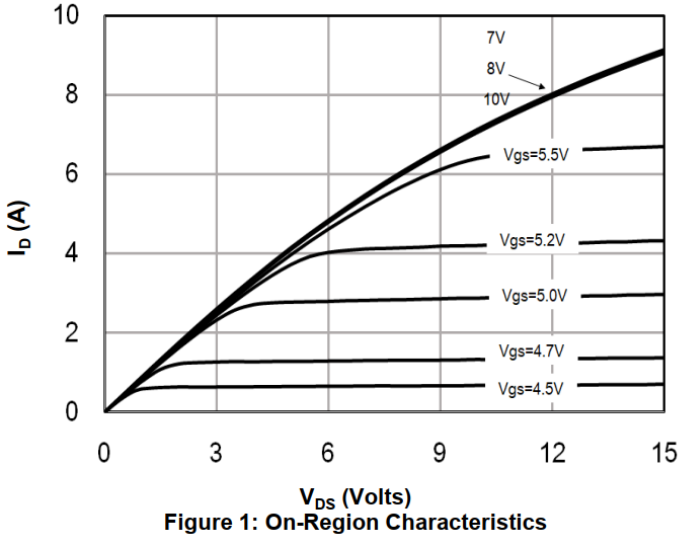


Figure 1: On-Region Characteristics

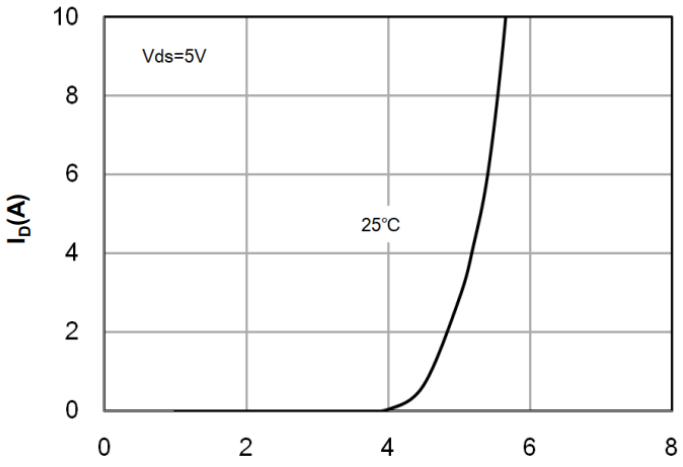


Figure 2: Transfer Characteristics

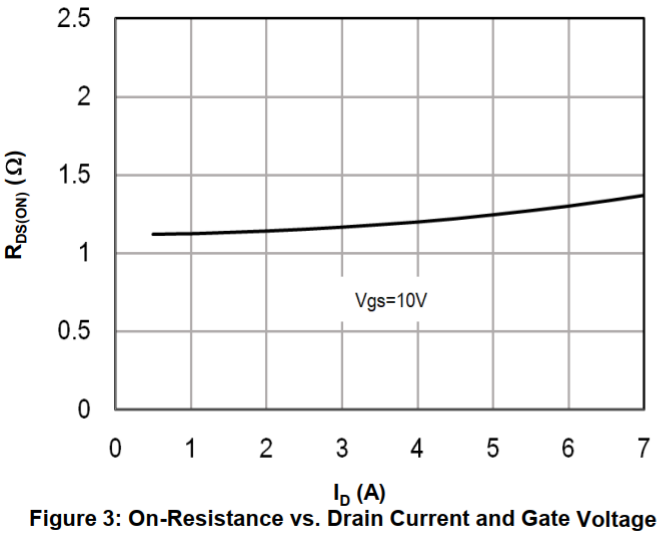


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

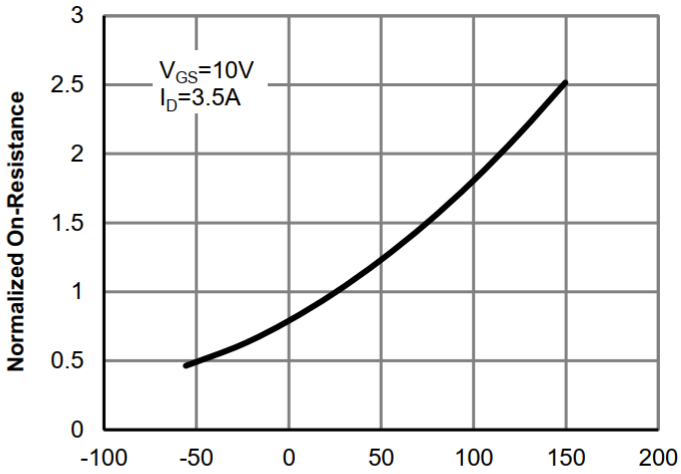


Figure 4: On-Resistance vs. Junction Temperature

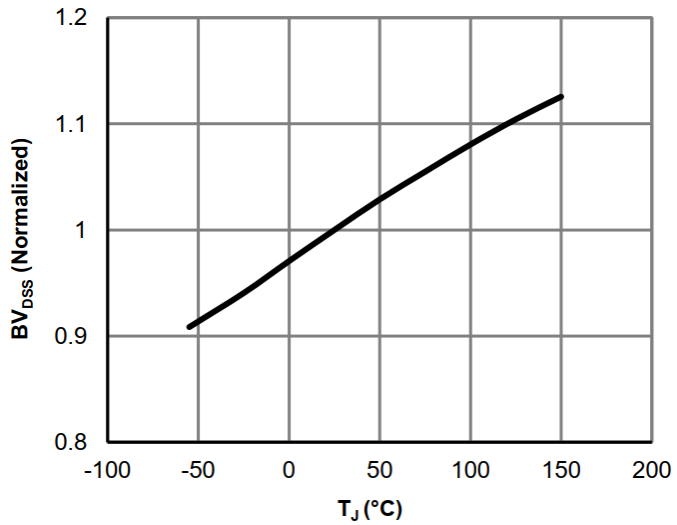


Figure 5: Break Down vs. Junction Temparature

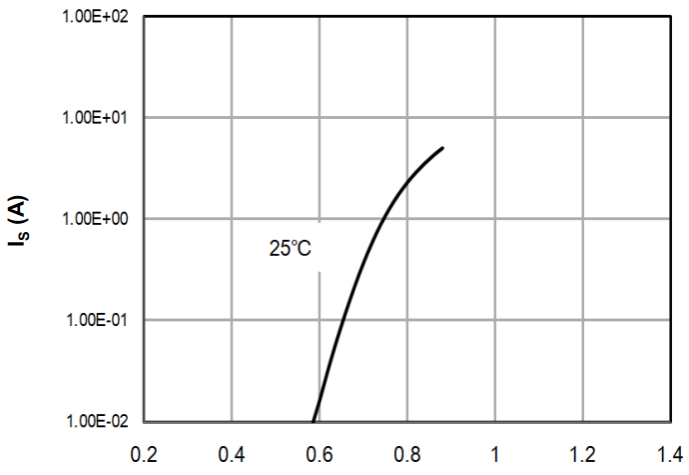


Figure 6: Body-Diode Characteristics

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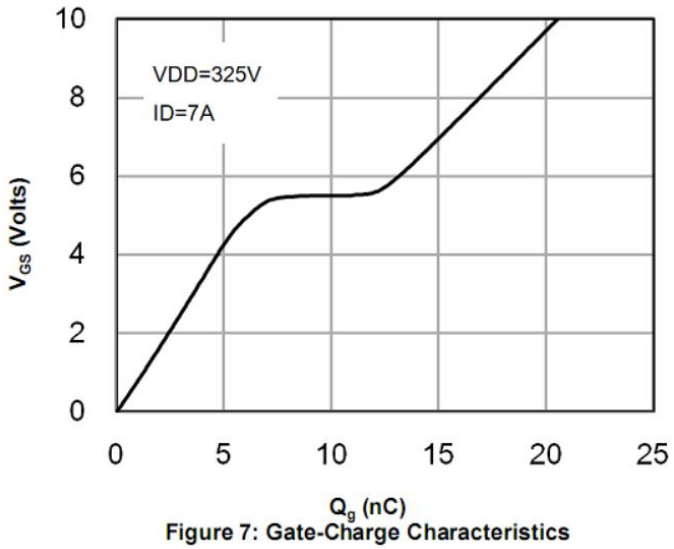


Figure 7: Gate-Charge Characteristics

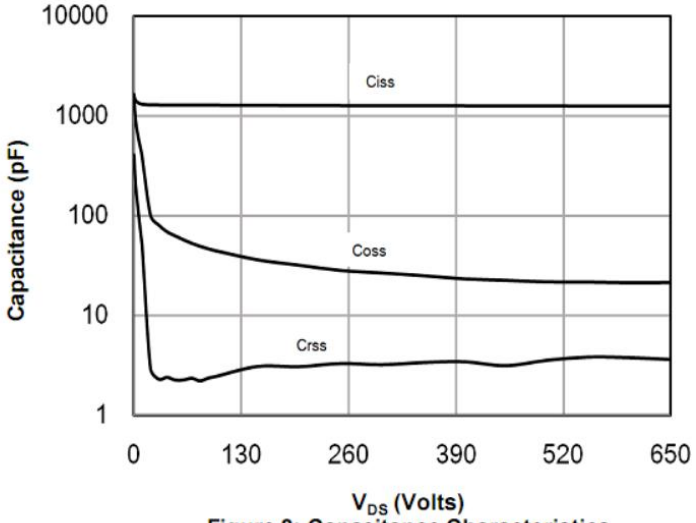


Figure 8: Capacitance Characteristics

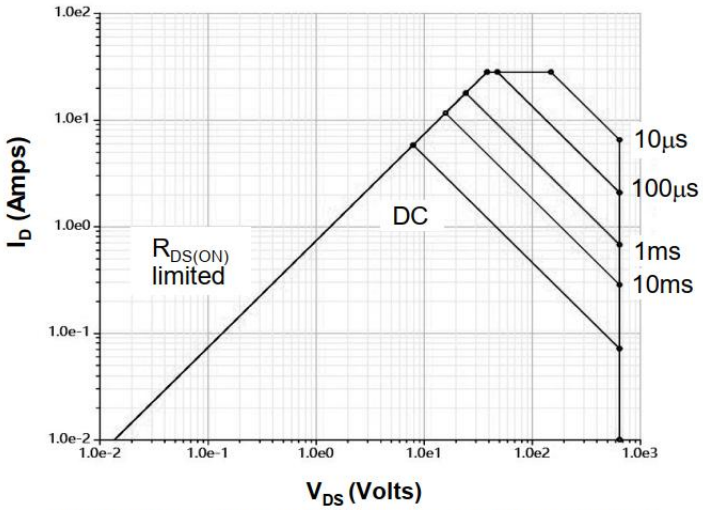


Figure 9: Maximum Forward Biased Safe Operating Area

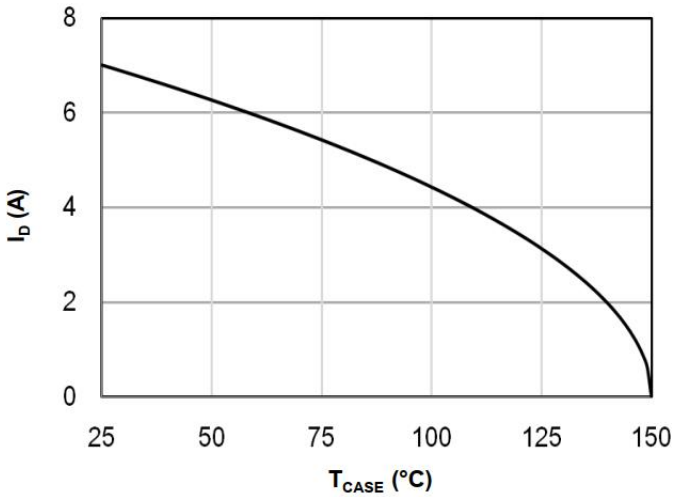


Figure 10: Tcase Temperature

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Test Circuits and Waveforms

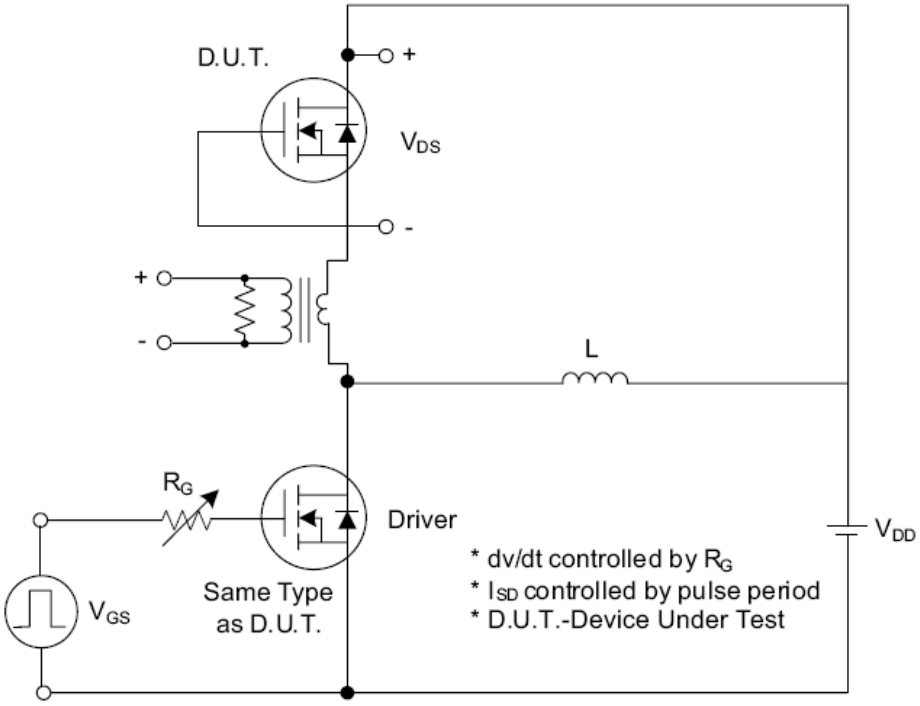


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

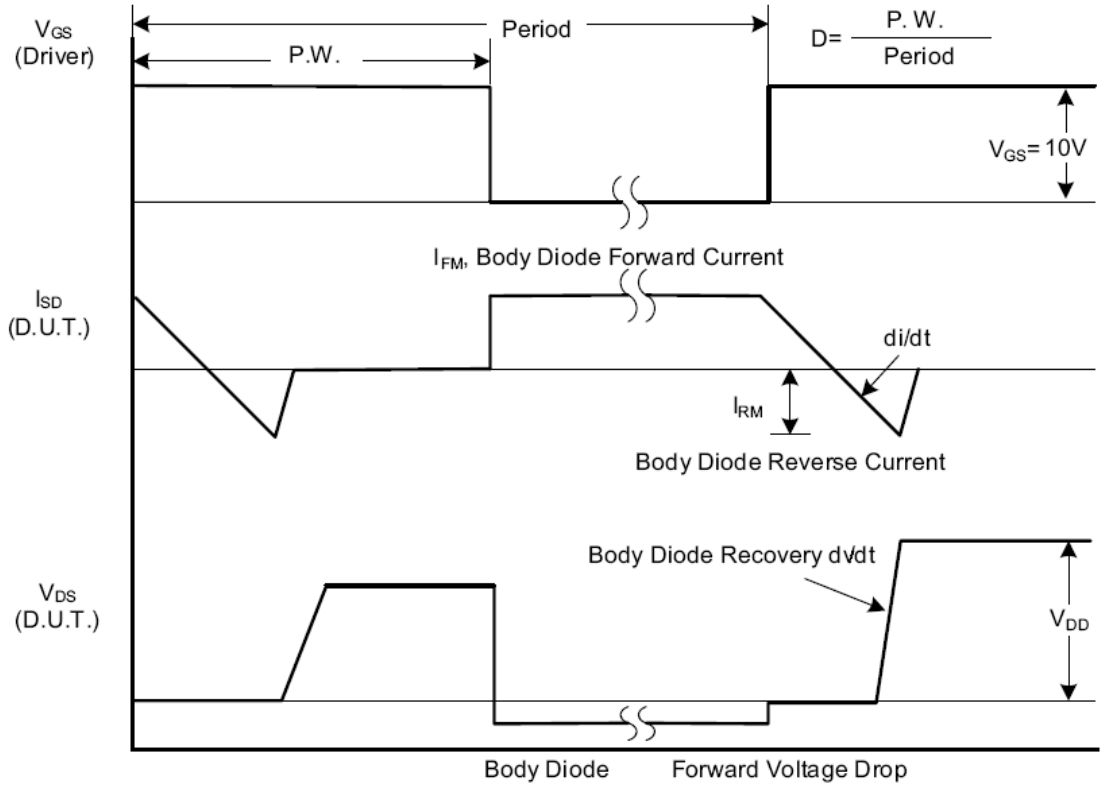


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

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Test Circuits and Waveforms (Cont.)

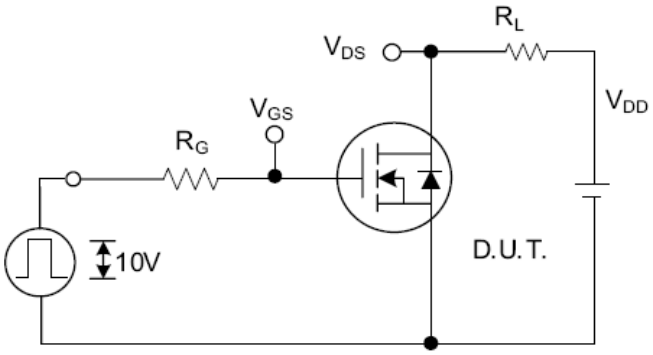


Fig. 2.1 Switching Test Circuit

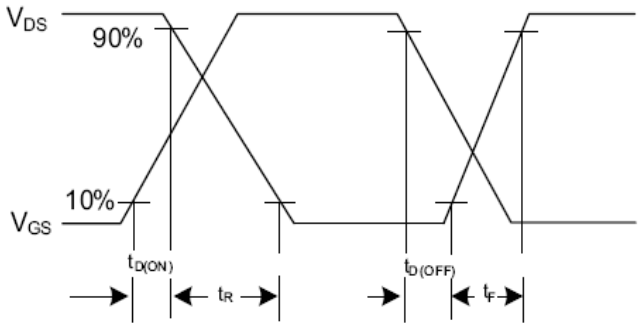


Fig. 2.2 Switching Waveforms

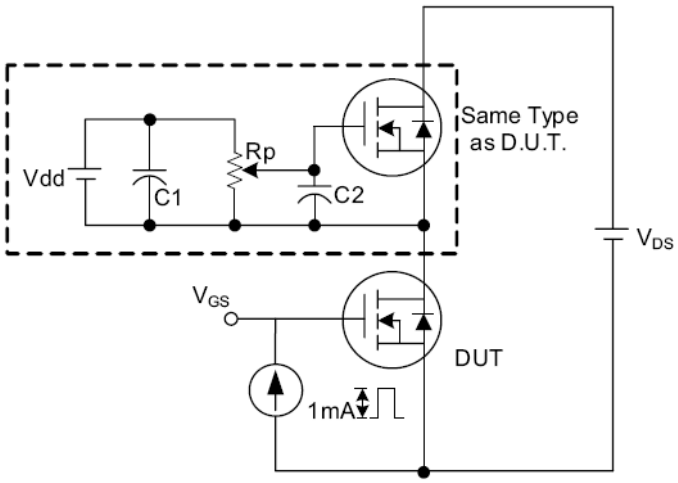


Fig. 3 . 1 Gate Charge Test Circuit

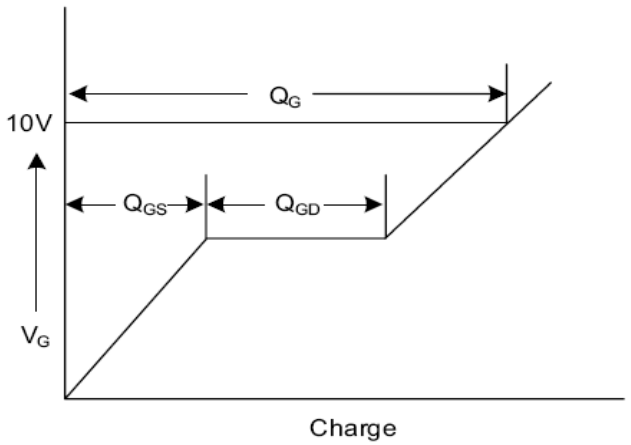


Fig. 3 . 2 Gate Charge Waveform

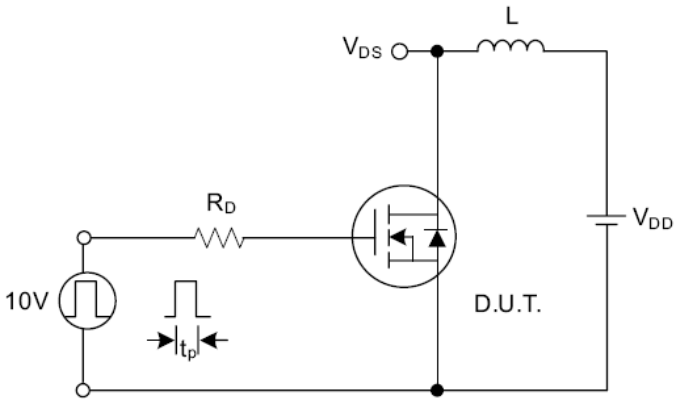


Fig. 4.1 Unclamped Inductive Switching Test Circuit

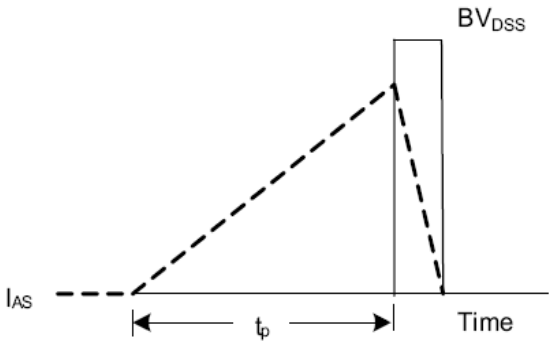


Fig. 4.2 Unclamped Inductive Switching Waveforms

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