650V N-ch Planar MOSFET

Lead Free Package and Finish

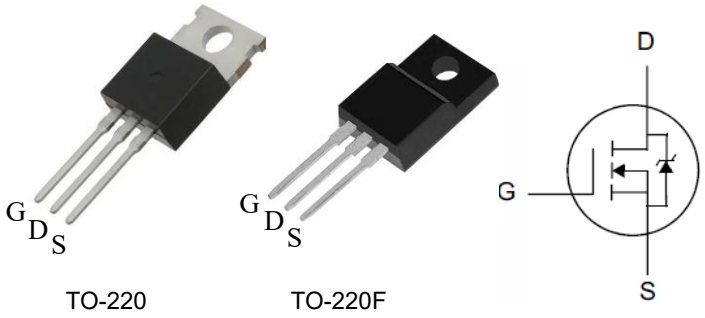
BV_{DSS}	$R_{DS(ON),typ.}$	I_D
650V	0.7Ω	10A

General Features

- RoHS Compliant
- $R_{DS(ON),typ.}$=0.7 Ω@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

Applications

- Adaptor
- Charger
- SMPS Standby Power



TO-220 TO-220F

Package No to Scale

Ordering Information

Part Number	Package	Brand
PTP10N65G	TO-220	
PTA10N65G	TO-220F	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	PTP10N65G	PTA10N65G	Unit
V_{DSS}	Drain-to-Source Voltage	650		V
V_{GSS}	Gate-to-Source Voltage	±30		
I_D	Continuous Drain Current	10		A
I_{DM}	Pulsed Drain Current at V_{GS}=10V	40		
E_{AS}	Single Pulse Avalanche Energy	800		mJ
P_D	Power Dissipation	125	45	W
	Derating Factor above 25℃	1.0	0.36	W/℃
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300		℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTP10N65G	PTA10N65G	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	2.78	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	62	

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Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	650	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=650V, V_{GS}=0V
		--	--	100		V_{DS}=520V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	0.7	0.85	Ω	V_{GS}=10V, I_D=5.0A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	2005	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	3.9	--		
C_{oss}	Output Capacitance	--	130	--		
Q_g	Total Gate Charge	--	32	--	nC	V_{DD}=520V, I_D=10A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	9	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	8.6	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	15	--	ns	V_{DD}=325V, I_D=10A, V_{GS}=10V Rg=4.7Ω
t_{rise}	Rise Time	--	3.4	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	24.5	--		
t_{fall}	Fall Time	--	10.8	--		

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Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current[2]	--	--	10	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current[2]	--	--	40		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=10A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	371	--	ns	V_{GS}=0V I_F= I_S, di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	2475	--	nC	

Note:

[1] T_J=+25℃ to +150℃
[2] Pulse width≤380μs; duty cycle≤2%.

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Typical Characteristics

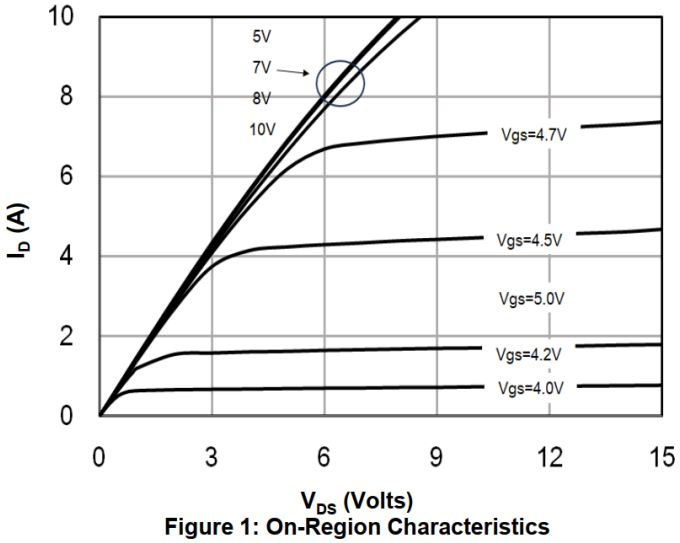


Figure 1: On-Region Characteristics

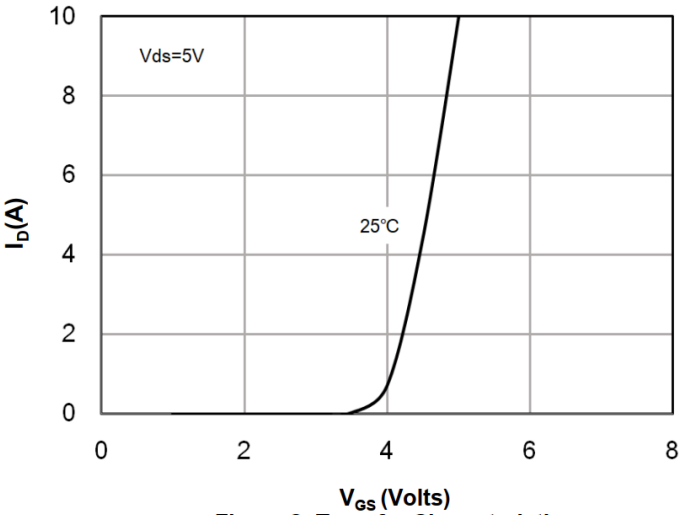


Figure 2: Transfer Characteristics

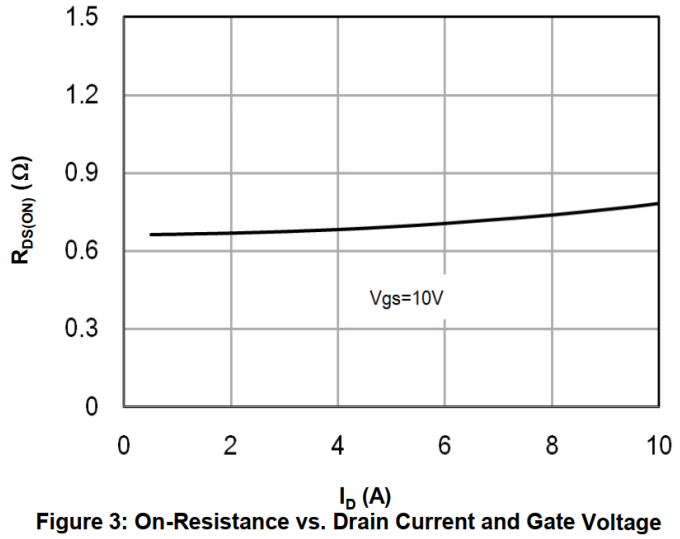


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

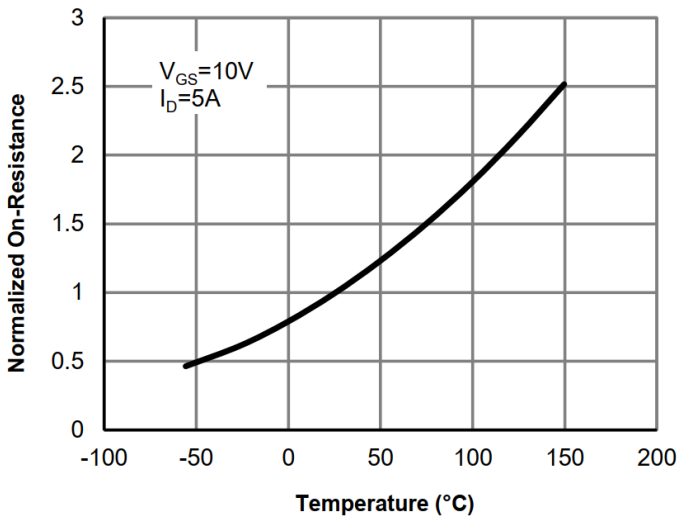


Figure 4: On-Resistance vs. Junction Temperature

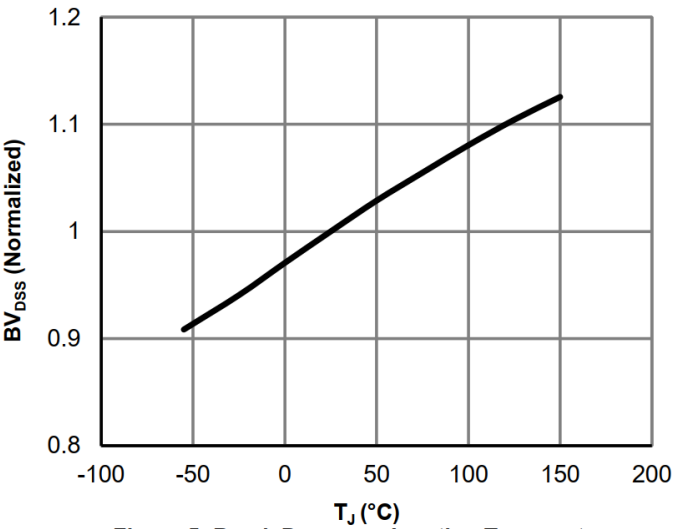


Figure 5: Break Down vs. Junction Temparature

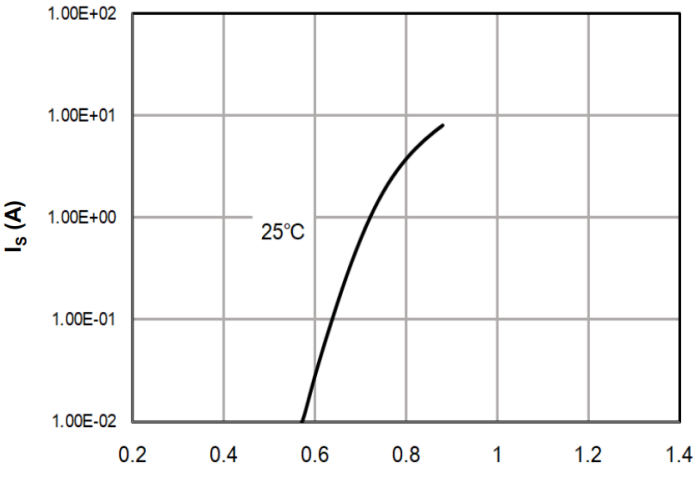


Figure 6: Body-Diode Characteristics

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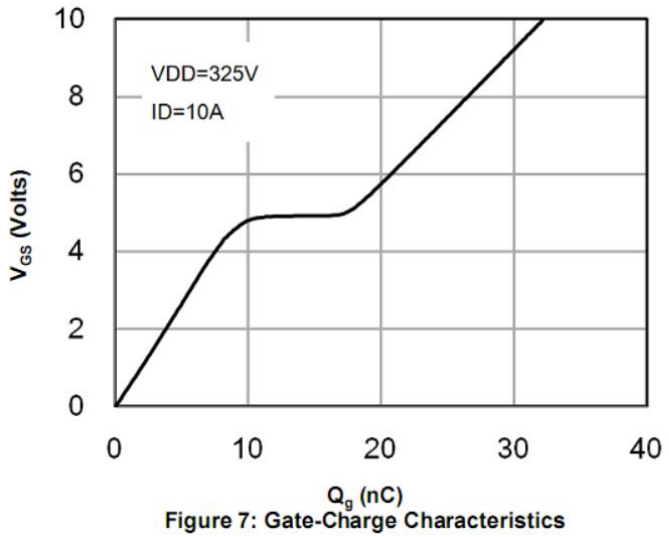


Figure 7: Gate-Charge Characteristics

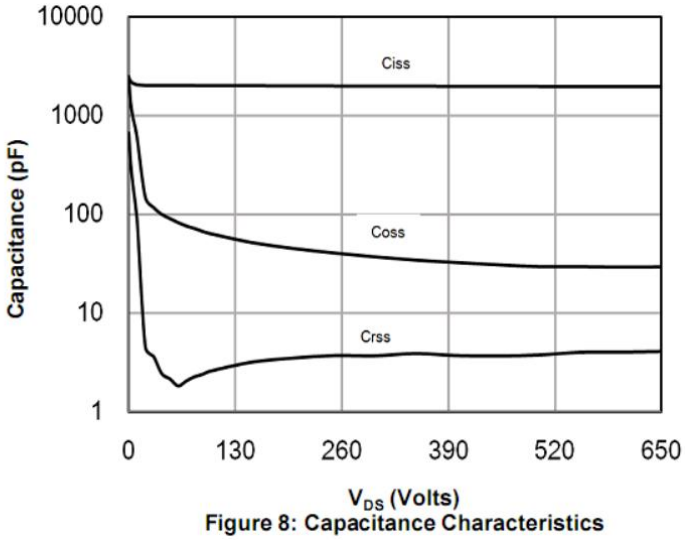


Figure 8: Capacitance Characteristics

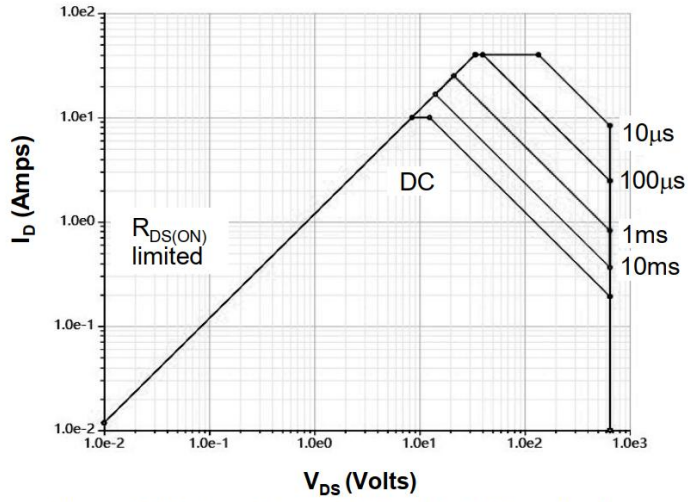


Figure 9: Maximum Forward Biased Safe Operating Area (TO-220)

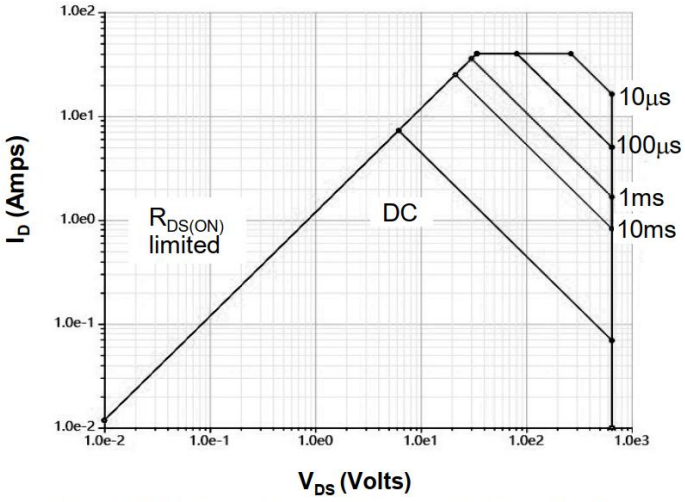


Figure 9: Maximum Forward Biased Safe Operating Area (TO-220F)

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Test Circuits and Waveforms

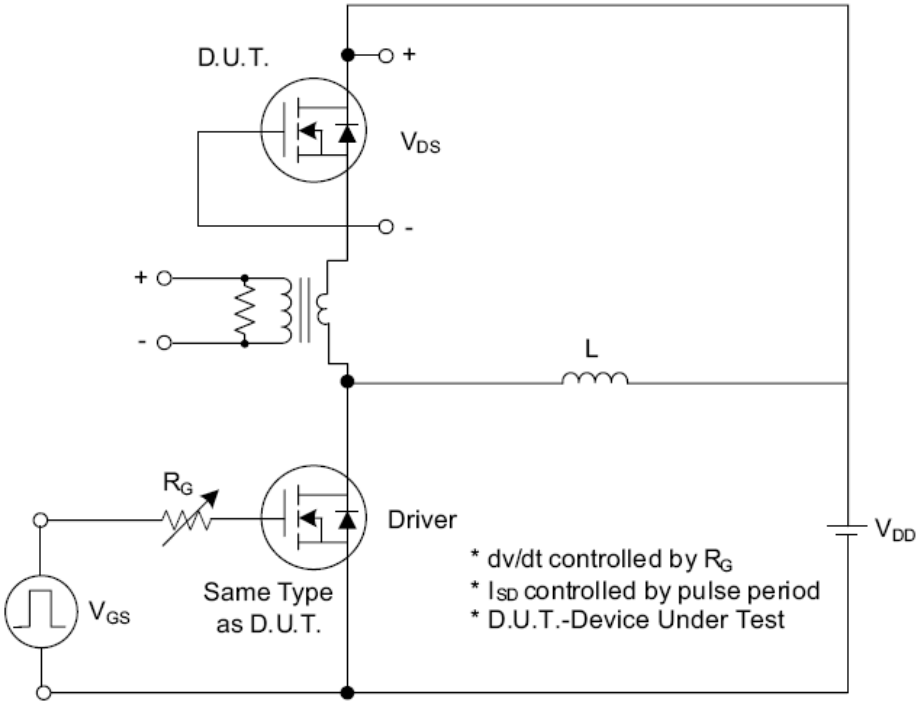


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

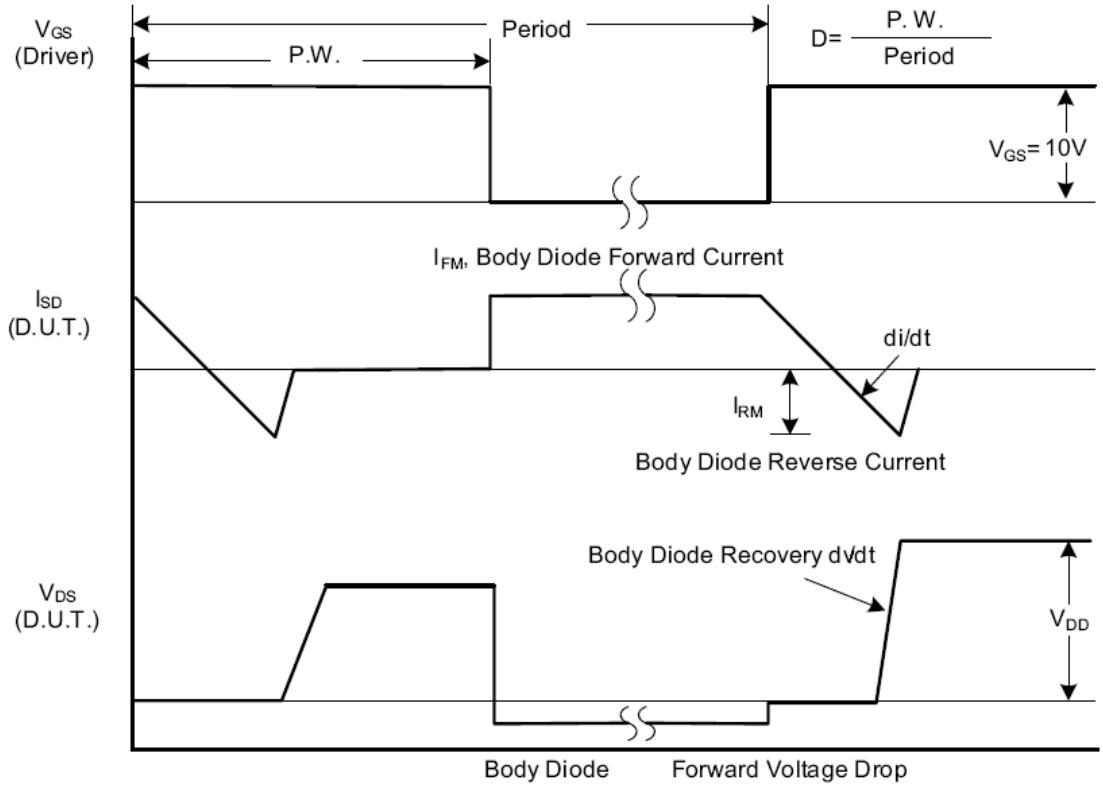


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

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Test Circuits and Waveforms (Cont.)

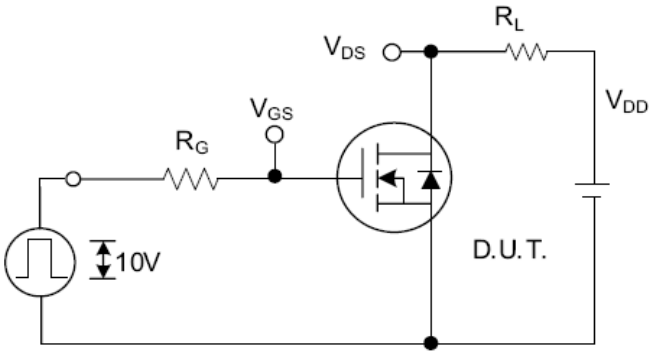


Fig. 2.1 Switching Test Circuit

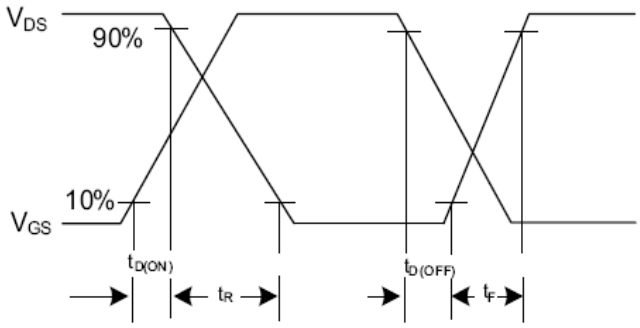


Fig. 2.2 Switching Waveforms

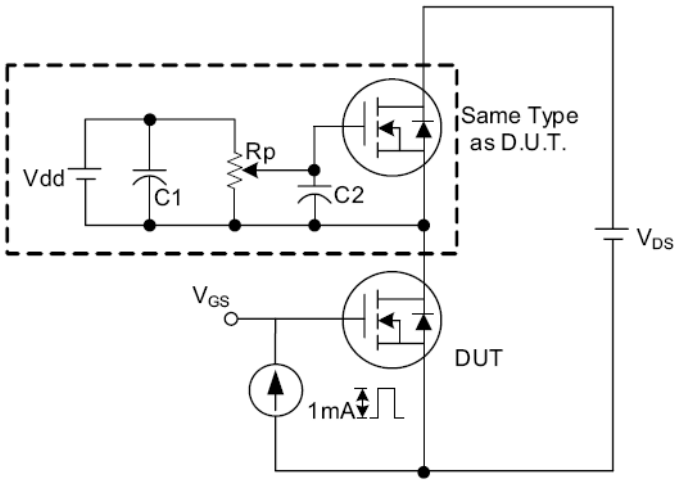


Fig. 3 . 1 Gate Charge Test Circuit

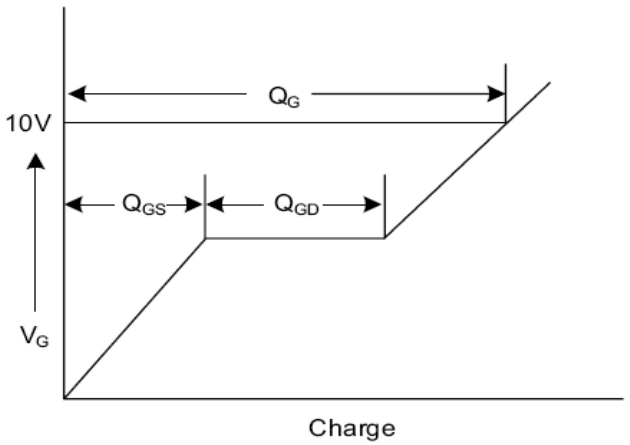


Fig. 3 . 2 Gate Charge Waveform

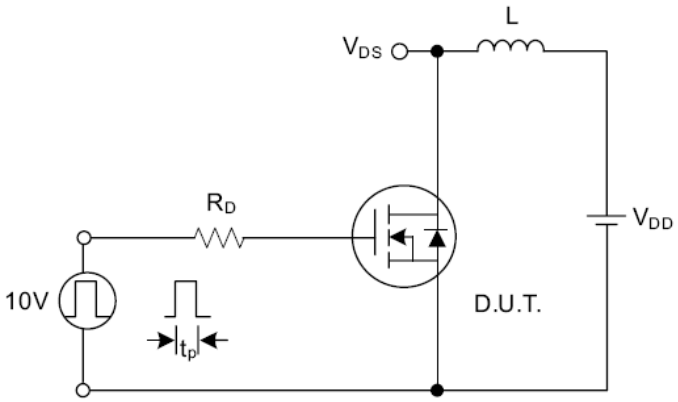


Fig. 4.1 Unclamped Inductive Switching Test Circuit

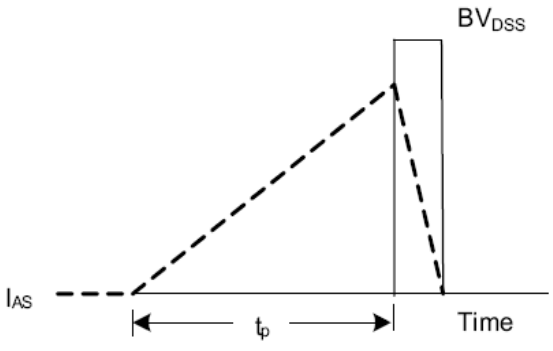


Fig. 4.2 Unclamped Inductive Switching Waveforms

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